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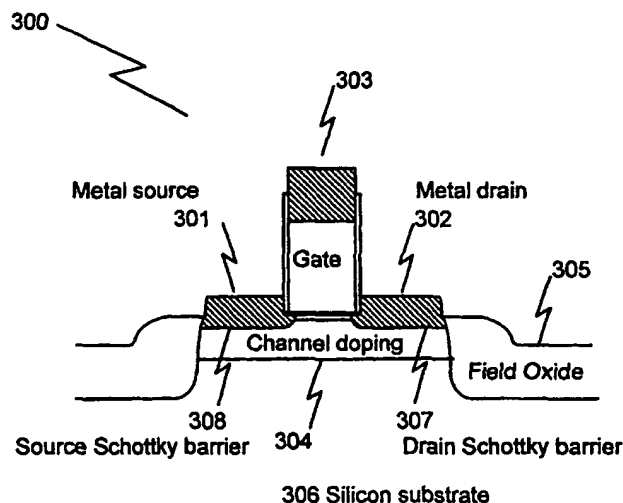
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(54) Title: MOSFET DEVICE SYSTEM AND METHOD



(57) Abstract: A MISFEED device system and method of fabricating same are disclosed. The present invention utilizes Schottky barrier contacts (301, 302) for source and/or drain contact fabrication within the context of a MISFEED device structure to eliminate the requirement for halo/pocket implants and shallow source/drain extensions to control short channel effects. Additionally, the present invention unconditionally eliminates the parasitic bipolar gain associated with MISFEED fabrication, reduces manufacturing costs, tightens control of device performance parameters, and provides for superior device characteristics as compared to the prior art.



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Title: MOSFET DEVICE SYSTEM AND METHOD**FIELD OF THE INVENTION**

The present invention relates generally to field of metal oxide semiconductor field effect transistors (MOSFETs), and has specific application to the fabrication of these devices in the context of an integrated circuit (IC).

BACKGROUND OF THE INVENTION

Since the invention of the transistor in the late 1940s, tremendous advances have been made in the field of microelectronics. Current technology allows for the cost-effective fabrication of integrated circuits (ICs) with over 100 million components - all on a piece of silicon roughly 10mm on a side. The one billion transistor IC will be commercially available within a few years. The desire for greater functionality and performance at less cost per IC drives several trends.

First, functionality drives IC transistor counts up. Second, the transistors themselves are being reduced in size so as to achieve greater packing density and, very importantly, to improve their performance. As far as performance is concerned, the key parameter for Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs, the dominant transistor technology of the day) is the channel length. The channel length (L) is the distance that charge carriers must travel to pass through the device, and a reduction in this length simultaneously implies higher current drives, reduced parasitic resistances and capacitances and improved high-frequency performance. A common figure-of-merit is the power-delay product, and this generalized measure of transistor performance improves as the cube of the inverse of the channel length ($1/L^3$). This explains the tremendous incentive that IC manufacturers have to reduce the channel length as much as manufacturing capabilities will allow.

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1 For digital applications, MOS transistors behave like switches. When 'on', they
drive relatively large amounts of current, and when turned 'off' they are characterized by
a certain amount of leakage current. As channel lengths are reduced, drive currents
increase, which is beneficial for circuit performance as stated above. However, leakage
currents increase as well. Leaky transistors contribute to quiescent power dissipation (the
6 power dissipated by an IC when idle) and in extreme cases can affect the transfer of
binary information during active operation. Device designers therefore have good reason
to keep leakage currents low as channel lengths are reduced.

MOS transistor leakage currents are traditionally controlled by introducing
controlled amounts of impurities (dopants) into the channel region of the device, and by
11 tailoring the source/drain lateral and vertical doping distributions. Although these
approaches are effective in shoring up the potential barrier internal to the MOS transistor
and therefore reducing the leakage current, they can also contribute to degraded drive
current and increased parasitic capacitance - the very items that channel length reduction
is meant to improve. Furthermore, depending on exactly how in the manufacturing
16 process the channel and tailored source/drain dopants are introduced, the manufacturing
cost can be affected significantly. Given traditional MOS transistor design and
architecture, there are only limited solutions to the trade-off between drive current,
leakage current, parasitic capacitance and resistance, and manufacturing complexity/cost.

The present invention offers a new relationship between these competing
21 requirements, and makes possible MOS devices with characteristics that are not achievable
with traditional (impurity doped) MOS architectures. The use of metal for the source and
drain and a simple, uniformly implanted channel dopant profile provides for improvements
to device characteristics in terms of reduced parasitic capacitance, reduced statistical

1 variations in these characteristics (especially as the channel length is decreased) and
reduced manufacturing cost and complexity.

DESCRIPTION OF THE PRIOR ART

Doping Profiles

Previous generations of MOS transistors have relied on laterally uniform, and
6 vertically non-uniform channel doping profiles to control drain-to-source leakage currents.
See Yuan Taur, "The Incredible Shrinking Transistor", IEEE SPECTRUM, pages 25-
29 (www.spectrum.ieee.org, ISSN 0018-9235, July 1999). FIG. 1 illustrates an exemplary
long-channel conventional MOS device (100) that comprises an impurity doped source
(101), an impurity doped drain (102), a conventional MOS type gate stack (103), and a
11 laterally uniform channel doping profile (104) in the substrate to assist in the control of
source-to-drain leakage currents. Devices are electrically isolated from each other via a
field oxide (105). Such channel dopant profiles are common in devices with channel
lengths down to approximately 200 nanometers (nm).

However, as device channel lengths have been reduced into the 100 nm regime the
16 literature teaches that channel doping profiles that are non-uniform in both the
lateral and vertical directions are required. Referencing FIG. 2, the exemplary short-
channel MOS device (200) has some elements similar to the long-channel MOS device
(100). The structure comprises a conventional impurity doped source (201) and drain
(202) as well as a conventional MOS gate stack (203) (width $< \sim 100$ nm, corresponding to
21 the channel length L). The structure further comprises shallow, impurity doped extensions
for the source (208) and drain (209) electrodes which are used in conjunction with drain
(206) and source (207) pocket doping as well as conventional channel doping (204) to
control source to drain leakage currents. Source and drain electrodes (201) and (202) and

1 their respective extensions (208) and (209) (the combination of all four of which comprise the tailored source/drain doping profile) are all of the same doping polarity (either N-type or P-type) and are of the opposite polarity from the channel (204) and pocket doping elements (206) and (207). Again, a field oxide (205) electrically isolates devices from each other.

6 In his paper entitled “**25 nm CMOS Design Considerations**” (1998 IEDM Technical Digest, page 789), Yuan Taur states

“ . . . an optimized, vertically and laterally non-uniform doping profile, called the super-halo, is needed to control the short channel effect.”

11 A similar statement has been made in the IEEE Spectrum magazine:

“ . . . in the 100 to 130 nm lithography generation, an optimally tailored profile that is both vertically and laterally non-uniform (Super-Halo) is need to control [short channel effects].”

16 See Linda Geppert, “**The 100-Million Transistor IC**”, IEEE SPECTRUM, pages 23-24 (www.spectrum.ieee.org, ISSN 0018-9235, July 1999).

Furthermore, virtually all the prior art that discusses device design for channel lengths less than 200 nm states or implies that channel doping profiles that are highly non-uniform in both the lateral and vertical directions are required for adequate control of drain-to-source leakage currents. For example, Hargrove in his paper “**High-Performance sub 0.08um CMOS with Dual Gate Oxide and 9.7 ps Inverter Delay** (1998 IEDM, page 627) states

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1 “In order to achieve optimal device performance . . . strong
 halos coupled with shallow junctions are required.”

The prior art is virtually unanimous in its statement that **laterally and vertically non-uniform doping profiles, in the form of laterally non-uniform channel dopants and shallow source/drain extensions, are required for adequate control of short channel effects.**

Pocket/Halo Implants

 Laterally non-uniform channel doping profiles are almost exclusively introduced after the gate electrode has been defined and is in place. With the gate serving as an implant mask, dopants of the same type as those already in the substrate are introduced
11 into the channel regions adjacent to the gate electrode’s edges via ion-implantation. As mentioned previously, these are often referred to as “pocket” or “halo” implants. See Yuan Taur, “**The Incredible Shrinking Transistor**”, IEEE SPECTRUM, page 28 (www.spectrum.ieee.org, ISSN 0018-9235, July 1999).

 While effective at reinforcing the electrostatic potential barrier between the source
16 and drain (and therefore reducing leakage currents), Halo/Pocket implants along with shallow source/drain extensions (the tailored source/drain doping profiles mentioned previously) add complexity to the manufacturing process. At least two additional lithography steps, as well as the associated cleans, implants, metrology, etc. are required to implement these process steps. As lithography is one of the most (if not the most)
21 expensive process modules in the production process, **this is a significant increase in manufacturing cost.** Halo and Pocket implants as well as shallow source/drain extensions can also add parasitic capacitance and a random statistical variation to device electrical characteristics.

1 Channel doping profiles for short channel Schottky MOS devices have received
only very limited attention in the prior art. J. R. Tucker discusses simulations done on
very short channel SBMOS devices and only mentions in passing that

“ . . . some doping of the semiconductor channel region will
be required in order to suppress (leakage) currents . . . ”.

6 See J. R. Tucker, C. Wang, J.W. Lyding, T. C. Shen, G. C. Abeln, “**Nanometer Scale
MOSFETs and STM Patterning on Si**,” SSDM 1994, pages 322-324; J. R. Tucker, C.
Wang, P.S. Carney, “**Silicon Field-Effect Transistor Based on Quantum Tunneling**,”
Applied Physics Letters, 1 Aug. 1994, Vol. 65, No. 5, pages 618-620. It is significant to
11 note that Tucker does not discuss in what manner one might go about introducing channel
doping to suppress source-to-drain leakage currents.

Q.T. Zhao is the next author to explicitly address the issue of **channel doping** to
control leakage currents. His approach (uniform doping of the substrate to quite high
levels ($10^{17}/\text{cm}^3$)) is well known to be non-optimal for short channel devices. Although he
16 is successful in reducing leakage currents, he does so at the expense of increased
source/drain-to-substrate capacitance. See Q.T. Zhao, F. Klinkhammer, M. Dolle, L.
Kappius, S. Mantl, “**Nanometer patterning of epitaxial $\text{CoSi}_2/\text{Si}(100)$ for ultrashort
channel Schottky barrier metal-oxide-semiconductor field effect transistors**,”
APPLIED PHYSICS LETTERS, Vol. 74 No. 3, 18 January 1999, page 454.

21 W. Saitoh reports on a device built on SOI substrates but does not discuss substrate
doping in this context. See W. Saitoh, S. Yamagami, A. Itoh, M. Asada, “**35 nm metal
gate SOI-P-MOSFETs with PtSi Schottky source/drain**,” Device Research Conference,
June 28-30, 1999, Santa Barbara, CA, Paper II.A.6, page 30.

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1 C. Wang mentions the use of “a layer of fully-depleted dopants beneath the active
region” and “preimplanting a thin subsurface layer of fully depleted dopants” to control
leakage currents, but does not describe the lateral uniformity or lack thereof of the doping
profile, or how one might go about producing the “layer”. See C. Wang, John P. Snyder, J.
R. Tucker, “**Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-**
6 **effect-transistors,**” APPLIED PHYSICS LETTERS, Vol. 74 No. 8, 22 Feb. 1999, pages
1174; C. Wang, John P. Snyder, J. R. Tucker, “**Sub-50 nm PtSi Schottky source/drain P-**
MOSFETs,” Annual Device Research Conference Digest 1998, pages 72-73.

Summary

Given the literature on substrate doping profiles for conventional short channel MOS transistors and the scant work on channel doping profiles for short channel Schottky MOS devices, the proposed invention offers a novel and non-obvious approach with many advantages over the current state-of-the-art.

OBJECTS OF THE INVENTION

Accordingly, the objects of the present invention are (among others) to circumvent the deficiencies in the prior art and affect one or more of the following objectives:

1. Provide a system and method to permit MOSFETs to be fabricated with short channel lengths with less cost, higher performance and better tolerances than current fabrication technologies.
2. Reduce parasitic bipolar operation in integrated MOSFETs, thus reducing the potential for latchup and other anomalous behavior.
3. Provide for MOSFET devices that have in some circumstances a higher degree of radiation hardness.

While these objectives should not be understood to limit the teachings of the present invention, in general these objectives are achieved by the disclosed invention that is discussed in the following sections.

BRIEF SUMMARY OF THE INVENTION

Overview

Referencing FIG. 3, an exemplary embodiment of the present invention (300) consists simply of a conventional MOS gate stack (303) (gate electrode on silicon dioxide on a silicon substrate), metal source (301) and/or drain (302) electrodes, and channel

1 dopants (304) that vary significantly in the vertical direction but not in the lateral
direction. A field oxide (305) electrically isolates devices from each other.

The Schottky (or Schottky-like) barriers (307, 308) that exist along the interface of
the corresponding metal source/drain (301, 302) and the silicon substrate (306) act as an
inherent pocket or halo implant and does so without added parasitic capacitance. It also
6 eliminates the need for shallow source/drain extensions as the metal source/drain is by its
nature shallow and highly conductive. Significant reductions in manufacturing complexity
are therefore achieved by simultaneous elimination of the halo/pocket implants and the
source/drain extensions. These are also major advantages over conventionally-architected-
channel MOS devices.

11 Due to the atomically abrupt nature of the Schottky barrier and the very consistent
and repeatable magnitude of this barrier, two sources of statistical variation which are
endemic to conventional MOS devices are virtually eliminated. The random statistical
nature of dopant introduction via ion-implantation in conventional devices produces
significant variations in the position and magnitude of implanted dopants. This is true for
16 both the halo/pocket and source/drain dopants. The result is a certain amount of random
variation in device parameters such as channel length (L), drive current, and leakage
current. These variations make circuit design more difficult and contribute to
manufacturing cost via yield loss due to ICs that do not meet performance specifications.
The problem becomes more severe as channel lengths are reduced due to the smaller
21 effective volume of silicon per device, and therefore less averaging to smooth away
statistical variations.

Because the metal source/drain (which replaces the conventional impurity doped
source/drain) has a natural, very consistent and atomically abrupt Scotty barrier (307, 308)

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1 with the silicon substrate (306) whose position and magnitude are independent of channel length, and because this barrier essentially plays the role of the halo/pocket implant (making these implants unnecessary), statistical variations due to random placement of atoms during the source/drain and halo/pocket implants are essentially eliminated. This fact remains true and even becomes more true as the channel length is reduced.

6 Another benefit of the metal source/drain MOS architecture is the **unconditional elimination of the parasitic bipolar gain**. The parasitic bipolar gain is a direct result of using opposite doping types for the source/drain and substrate regions, and can result in latch-up and other deleterious effects. When the source/drain electrodes are constructed of metal, this parasitic gain is eliminated. This makes the metal source/drain architecture
11 ideal for (among other things) high-radiation environments.

General Advantages

The present invention typically provides the following benefits as compared to the prior art:

1. Reduction in manufacturing complexity. Pocket/Halo implants and shallow
16 source/drain extensions are not needed.
2. Reduction in capacitance due to absence of pocket/halo implants.
3. Reduction in random/statistical variations of device electrical characteristics due to absence of pocket/halo implants and source/drain extensions, and the use of metal for the source and drain.
- 21 4. Unconditional elimination of the parasitic bipolar gain and associated latchup.
5. Increased radiation hardness as compared to conventional MOS structures.

The above list of advantages should not be interpreted as to limit the scope of the present invention. However, one skilled in the art will recognize a plethora of application

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1 opportunities for the present invention teachings given the above-mentioned list of general advantages that are potentially available.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the advantages provided by the invention, reference should be made to the following detailed description together with the accompanying
6 drawings wherein:

FIG. 1 illustrates a prior art long channel, impurity doped source/drain device;

FIG. 2 illustrates a prior art short channel, impurity doped source/drain device with pocket implants and source/drain extensions;

FIG. 3 illustrates an exemplary embodiment of the present invention as applied to a
11 short channel, metal source/drain device without pocket implants;

FIG. 4 illustrates an exemplary embodiment of the present invention process fabrication step using an implanted silicon substrate with approximately 200 Å screen oxide;

FIG. 5 illustrates an exemplary embodiment of the present invention process
16 fabrication step using a patterned in-situ doped silicon film on thin gate oxide;

FIG. 6 illustrates an exemplary embodiment of the present invention process fabrication step using a formation of thin oxide sidewalls, and exposure of silicon in the gate, source and drain areas;

FIG. 7 illustrates an exemplary embodiment of the present invention process
21 fabrication step using a metal deposition and solidification anneal.

FIG. 8 illustrates an exemplary embodiment of the present invention process fabrication step using a removal of unreacted metal from the sidewalls;

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1 FIG. 9 illustrates an exemplary embodiment of the present invention process
fabrication resulting structure. In-situ phosphorous doped silicon, Erbium silicide and
Indium channel implants are used for the N-type device for the gate electrode, source/drain
electrodes and channel doping respectively. The P-type devices make use of in-situ Boron
doped silicon, Platinum Silicide and Arsenic channel implants. The channel dopant
6 concentrations vary significantly in the vertical direction but not in the lateral direction.
Gate lengths are typically <100 nm, but may be longer;

 FIG. 10 illustrates an exemplary general system process flowchart showing a
method of producing superior MOSFET devices;

 FIG. 11 illustrates an exemplary detailed system process flowchart showing a
11 method of producing superior MOSFET devices.

DESCRIPTION OF THE PRESENTLY PREFERRED EXEMPLARY EMBODIMENTS

Embodiments are Exemplary

16 While this invention is susceptible of embodiment in many different forms, there is
shown in the drawings and will herein be described in detailed preferred embodiment of
the invention with the understanding that the present disclosure is to be considered as an
exemplification of the principles of the invention and is not intended to limit the broad
aspect of the invention to the embodiment illustrated.

21 The numerous innovative teachings of the present application will be described
with particular reference to the presently preferred embodiments, wherein these innovative
teachings are advantageously applied to the particular problems of a MOSFET DEVICE
SYSTEM AND METHOD. However, it should be understood that these embodiments are
only examples of the many advantageous uses of the innovative teachings herein. In

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1 general, statements made in the specification of the present application do not necessarily
limit any of the various claimed inventions. Moreover, some statements may apply to
some inventive features but not to others. In general, unless otherwise indicated, singular
elements may be in the plural and visa versa with no loss of generality.

Definitions

6 Throughout the discussion in this document the following definitions will be
utilized:

System Blocks/Procedural Steps Not Limitive

The present invention may be aptly described in terms of exemplary system block
diagrams and procedural flowcharts. While these items are sufficient to instruct one of
11 ordinary skill in the art the teachings of the present invention, they should not be strictly
construed as limiting the scope of the present invention. One skilled in the art will be
aware that system block diagrams may be combined and rearranged with no loss of
generality, and procedural steps may be added or subtracted, and rearranged in order to
achieve the same effect with no loss of teaching generality. Thus, it should be understood
16 that the present invention as depicted in the attached exemplary system block diagrams and
procedural flowcharts is for teaching purposes only and may be reworked by one skilled in
the art depending on the intended target application.

Predetermined Regions

21 Throughout the following discussion the term 'predetermined region' will be
defined to encompass the area centered at the heart of the active device (MOSFET). Thus,
all the process steps mentioned in the context of a MOSFET will create a gate,
source/drain, and/or channel doping profiles as well as other structures in an area proximal

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1 to the predetermined regions or heart of the active device. The present invention places no restrictions on what occurs outside this context, far from the heart of the active device.

It should be noted that while the predetermined region will generally be spoken of in terms of a MOSFET device, this in no way limits the scope of the present invention.

One skilled in the art will recognize that any device capable of regulating the flow of
6 electrical current may be considered to have a predetermined region in proximity to its active current carrying region.

MOSFET Not Limitive

The present invention is particularly suitable for use with MOSFET semiconductor devices, but the use of the present teachings is not limited to this particular application.

11 Other semiconductor devices, whether integrated or not, may be applied to the present invention teachings. Thus, while this specification speaks in terms of 'MOSFET' devices, this term should be interpreted broadly to include any device for regulating the flow of electrical current having a conducting channel that has two or more points of electrical contact.

Channel Length Not Limitive

16 The present invention is particularly suitable for use in situations where short channel length MOSFETs are to be fabricated, especially in the range of channel lengths <100 nm. However, nothing in the teachings of the present invention limits application of the teachings of the present invention to these short channel length devices. Advantageous
21 use of the teachings of the present invention may be had with channel lengths of any dimension.

Dopants Not Limitive

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1 Throughout the discussion herein there will be examples provided that utilize various dopant technologies in regards to MOSFET device fabrication. These dopants are only illustrative of a specific embodiment of the present invention and should not be interpreted to be Limitive of the scope of teachings within the current invention.

6 Note, however, that the present invention specifically anticipates the use of impurity atoms are selected from the group consisting of Arsenic, Phosphorous, Antimony, Boron, Indium, and/or Gallium as being within the scope of the teachings of the present invention.

Device Type Not Limitive

11 One skilled in the art will readily realize that the present invention is not limited in scope to either N-type or P-type devices but may be used with either or both device types.

Source/Drain Not Limitive

16 Throughout the discussion herein there will be examples provided that make reference to 'source' and 'drain' connections in regards to MOSFET device fabrication. One skilled in the art will recognize that in any given MOSFET configuration the nomenclature surrounding these contacts may be swapped without loss of generality, so that the 'source' may be interchanged with the 'drain' contact with no loss in the scope of the present invention. Additionally, one skilled in the art will recognize that while many preferred embodiments of the present invention may be used to fabricate **both** source and drain connections, there is no requirement that this be the case in actual practice. One, 21 both, or none of the source/drain connections on a given device in the context of an IC or the like may use the teachings of the present invention to advantage.

Thus, the terms 'source' and 'drain' should be interpreted to include the variants 'drain' and 'source' as well as 'source or drain' and 'source and drain'.

1 **Metals Not Limitive**

Throughout the discussion herein there will be examples provided that make reference to metals in regards to MOSFET device fabrication. The present invention does not recognize any limitations in regards to what types of metals may be used in affecting the teachings of the present invention. Thus, metals commonly used at the transistor level
6 such as titanium, cobalt and the like are specifically anticipated, as well as a plethora of more exotic metals and other alloys. Nothing in the disclosure limits the use of the invention with any particular metal or alloy. One skilled in the art will recognize that any conductive interconnecting material may be used with no loss of generality in implementing the teachings of the present invention.

11 Note, however, that the present invention specifically anticipates the use of source/drain electrodes formed from the group consisting of any of Platinum Silicide, Palladium Silicide, Iridium Silicide, and/or the rare-earth silicides as being within the scope of the teachings of the present invention.

Schottky Not Limitive

16 Throughout the discussion herein there will be examples provided that make reference to 'Schottky' barriers and like contacts in regards to IC fabrication. The present invention does not recognize any limitations in regards to what types of Schottky interfaces may be used in affecting the teachings of the present invention. Thus, the present invention specifically anticipates these types of junctions to be created with any form of
21 conductive material.

Additionally, while traditional Schottky junctions are abrupt, the present invention specifically anticipates that in some circumstances an **interfacial layer** may be utilized between the silicon substrate and the actual Schottky barrier metal. Thus, the present

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1 invention specifically anticipates 'Schottky-like' junctions and their equivalents to be
useful in implementing the present invention. Furthermore, the interfacial layer may
comprise materials that have conductive, semi-conductive, and/or insulator-like properties.

Etching Technology Not Limitive

6 Throughout the discussion herein there will be examples provided that make
reference to a variety of etching technologies utilized to remove oxide and/or metal in the
IC fabrication process. The present invention does not restrict the type of etching
technology used to achieve the results illustrated in the typical process flows. These
etching technologies are well known in the art.

Process/Method

11 One possible process flow for the fabrication of channel implanted, short channel
($<100\text{nm}$) metal source/drain MOS devices (400) is illustrated in FIGS. 4-9. While this
exemplary process flow is just exemplary of the broad teachings of the present invention, it
will prove very instructive to one skilled in the art to teach the fundamental concepts of the
present invention. This exemplary process flow may be described as follows:

- 16 1. Referencing FIG. 4, starting with a silicon substrate (402) that has means for
electrically isolating transistors from one another, a thin screen oxide (401) is
grown (approximately 200 \AA) to act as an implant mask. The appropriate channel
dopant species (403) (for example Arsenic and Indium for P-type and N-type
devices respectively) is then ion-implanted through the screen oxide to a pre-
21 determined depth in the silicon (approximately 1000 \AA or so).
2. Referencing FIG. 5, the screen oxide is then removed in hydro-fluoric acid, and a
thin gate oxide (501) (approximately 35 \AA) is grown. The gate oxide growth is
immediately followed by an in-situ doped silicon film. The film is heavily doped

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1 with, for example, Phosphorous for an N-type device and Boron for a P-type device. Using lithographic techniques and a silicon etch that is highly selective to oxide, the gate electrode (502) is patterned as shown in the process step (500) illustrated in FIG. 5.

3. A thin oxide (approximately 100 Å) is then thermally grown on the top surface and
6 sidewalls of the silicon gate electrode. Referencing FIG. 6, an anisotropic etch is then used to remove the oxide layers on the horizontal surfaces (and thus expose the silicon (601)), while preserving them on the vertical surfaces. In this way, a sidewall oxide (602) is formed, and the dopants both in the gate electrode and in the channel region of the device are electrically activated as shown in the process
11 step (600) illustrated in FIG. 6.

4. Referencing FIG. 7, the final step encompasses depositing an appropriate metal (for example, Platinum for the P-type device and Erbium for the N-type device) as a blanket film (approximately 400 Å) on all exposed surfaces. The wafer is then annealed for a specified time at a specified temperature (for example, 400°C for
16 45 minutes) so that, at all places where the metal is in direct contact with the silicon, a chemical reaction takes place that converts the metal to a metal silicide (701). The metal that was in direct contact with a non-silicon surface (702) is left unaffected as shown in the process step (700) illustrated in FIG. 7.

5. A wet chemical etch (aqua regia for Platinum, HNO₃ for Erbium) is then used to
21 remove the unreacted metal while leaving the metal-silicide untouched. The channel implanted, short channel Schottky barrier MOS device is now complete and ready for electrical contacting to gate, source, and drain as shown in the process step (800) illustrated in FIG. 8.

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1 This process is only one possible way to achieve channel implanted, metal
source/drain Schottky MOS devices. One skilled in the art will recognize that many other
variants and alternatives exist.

Device/System

FIG. 9 shows a preferred exemplary embodiment of the invention, as exemplified
6 by two final complementary MOSFET structures (900). This embodiment consists of N-
channel devices fabricated with Erbium Silicide (904) for the source/drain regions, and a
P-channel device fabricated with Platinum Silicide (905).

Vertically varying, laterally non-varying Indium (902) and Arsenic (903) layers are
used as the channel dopants for the N-channel and P-channel devices respectively. These
11 dopant atoms are used due to their relatively low rates of diffusion through the silicon
lattice (compared to Phosphorous and Boron, the other two possible candidates for channel
dopants). This allows for greater thermal budget during fabrication of the device, and
therefore less statistical variation in the characteristics of the finished product.

The gate electrodes are fabricated from in-situ Phosphorous and Boron doped
16 polysilicon films for the N-type (906) and P-type (907) devices respectively. In this
instance, Phosphorous and Boron are used due to their large solid-solubilities (compared to
Arsenic and Indium). The electrodes are doped via the use of an in-situ method, wherein
the impurity atoms are deposited at the same time the silicon atoms are. Such a method
can achieve very large doping concentrations (approximately $10^{21}/\text{cm}^3$) and a uniform
21 distribution throughout the thickness of the film. Another option for doping the silicon
gate is ion-implantation. This method suffers from several practical problems including
charging damage to the thin gate oxide, and the need to redistribute the highly non-uniform
as-implanted gate dopants to achieve high doping levels at the gate oxide interface.

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1 The gate electrodes (906) and (907) are less than 100 nm in width (corresponding to the channel length L), as it is in this regime that the advantages of the Schottky barrier architecture over the conventional architecture become apparent. These include simplified processing due to the absence of need for pocket implants, and the resulting reduction in yield loss, capacitance and statistical variations in finished products.

6 Devices are separated from each other by a thermally grown oxide (called a Field Oxide) (901) that works in conjunction with the channel dopants to electrically isolate the devices from each other.

 While the above description contains many specifics, these should not be construed as limitations on the scope of the invention, but rather as an exemplification of one
11 preferred embodiment thereof. One skilled in the art will realize that many other variations are possible. For example, there are many possible candidates for the source/drain metal. It may also be advantageous to insert a thin oxide layer between the metal and the silicon substrate. The silicon substrate itself may be replaced by any number of other semiconductors. Additionally, boundaries between layers or elements can always
16 be graded or interposed with other materials or interface agents to improve performance.

Generalized Process/System Fabrication

 From the foregoing discussion, the process and system embodied in the present invention may be further generalized as illustrated in the flowcharts shown in FIGs. 10-11.

Generalized Process/System

21 Referencing FIG. 10, an exemplary generalized MOSFET device process fabrication flow (1000) starts with a semiconductor substrate having means for electrically isolating transistors (1000). On this substrate, channel dopants are introduced in such a way that the dopant concentration varies significantly in the vertical but not the lateral

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1 direction (1002). Once this is complete, a gate electrode is formed (1003) on the silicon
substrate. Finally, source and/or drain electrodes are formed, at least one of which
incorporates a Schottky or Schottky-like contact to the semiconductor substrate (1004).

Detailed Process/System

Referencing FIG. 11, an exemplary detailed MOSFET device process fabrication
6 flow (1100) starts with a semiconductor substrate having means for electrically isolating
transistors (1101). On this substrate, channel dopants are introduced in such a way that the
dopant concentration varies significantly in the vertical but not the lateral direction (1102).
Once this is complete, a gate electrode insulator is formed by growing a thin gate
insulating layer and depositing a conducting film (1103) on the silicon substrate.

11 At this point a series of pattern and etching steps are performed to form a gate
electrode (1104). Then one or more thin insulating layers are formed on one or more
sidewalls of the gate electrode to selectively expose the semiconductor substrate on the
active areas of the device except for the sidewalls (1105). A thin film of metal is deposited
on all surfaces of the device (1106), and the device is thermally annealed to form a metal-
6 semiconductor alloy on the exposed semiconductor surfaces (1107). Finally, unreacted
metal is removed from the device while leaving the metal-semiconductor alloy untouched
to form local interconnect for the formed device (1108).

Summary

11 In substance, the present invention may be summarized by noting that the basic
structure is one in which the substrate between the source and drain is uniformly doped in
the lateral direction, non-uniformly doped in the vertical direction, and that the source
and/or drain electrodes form Schottky or Schottky-like contacts with the substrate.

CONCLUSION

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1 A short channel length, laterally uniform doped channel, metal source and
drain MOS device structure and method for manufacture has been disclosed. The
present invention provides for many advantages over the prior art including lower
manufacturing costs, superior device characteristics, and tighter control of device
parameters. These advantages are achieved primarily through the introduction of a
6 channel doping profile that is both laterally uniform and vertically non-uniform, in
conjunction with metal source/drain regions, thus eliminating the need for halo/pocket
implants and shallow source/drain extensions. The parasitic bipolar gain is
unconditionally eliminated as well.

 These features of the invention make it ideal for many applications, including but
1 not limited to high frequency and/or high radiation environments.

1 CLAIMS

Although a preferred embodiment of the present invention has been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

What is claimed is:

1. A MOSFET device comprising:

- (1) a source connection;
- (2) a drain connection;
- (3) a substrate between said source and said drain connections, said substrate being laterally uniformly doped and vertically non-uniformly doped;

wherein

said source and/or said drain connections form a

Schottky barrier connection to said substrate.

- 2. The MOSFET device of Claim 1 wherein the length of said substrate is less than or equal to 100 nm.
- 3. The MOSFET device of Claim 1 wherein said source connection and/or said drain connections incorporate an interfacial layer within said Schottky barrier.
- 4. The MOSFET device of Claim 3 wherein the length of said substrate is less than or equal to 100 nm.
- 5. A MOSFET device comprising:
 - (1) a source connection means;
 - (2) a drain connection means;

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1 (3) a substrate means between said source and said drain connection means,
 said substrate means being laterally uniformly doped and vertically non-
 uniformly doped;

 wherein

 said source and/or said drain connection means form a

6 Schottky barrier connection to said substrate
 means.

6. The MOSFET **device** of Claim 5 wherein the length of said substrate means is less
 than or equal to 100 nm.

7. The MOSFET **device** of Claim 5 wherein said source connection means and/or said
11 drain connection means incorporates an interfacial layer within said Schottky
 barrier means.

8. The MOSFET **device** of Claim 7 wherein the length of said substrate means is less
 than or equal to 100 nm.

9. A **device** for regulating the flow of electrical current comprising:

6 (1) a semiconductor substrate;

 (2) a gate electrode;

 (3) source and drain electrodes which, at least at some point proximal to either
 edge of said gate electrode, form a Schottky or Schottky-like interface with
 said semiconductor substrate;

11 (4) impurity atoms embedded within said semiconductor substrate and being
 distributed, at least in the region proximal to said gate electrode, so that the
 concentration of said impurity atoms does not vary substantially in the
 direction parallel to said surface of said semiconductor substrate, but does

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- 1 vary substantially in the direction perpendicular to said surface of said
semiconductor substrate.
10. The **device** of Claim 9 wherein said source electrode and/or said drain electrode
incorporates an interfacial layer within said Schottky and/or said Schottky-like
barrier.
- 6 11. The **device** of Claim 9 wherein said source and/or drain electrodes are formed from
the group consisting of Platinum Silicide, Palladium Silicide and Iridium Silicide,
and said impurity atoms are selected from the group consisting of Arsenic,
Phosphorous and Antimony.
- 11 12. The **device** of Claim 9 wherein said source and/or drain electrodes are formed from
the group consisting of any of the rare-earth silicides, and said impurity atoms are
selected from the group consisting of Boron, Indium and Gallium.
13. The **device** of Claim 9 wherein said gate electrode has a width not exceeding 100
nm.
- 6 14. The **device** of Claim 13 wherein said source and/or drain electrodes are formed
from the group consisting of Platinum Silicide, Palladium Silicide and Iridium
Silicide, and said impurity atoms are selected from the group consisting of Arsenic,
Phosphorous and Antimony.
15. The **device** of 13 wherein said source and/or drain electrodes are formed from the
group consisting of any of the rare-earth silicides, and said impurity atoms are
1 selected from the group consisting of Boron, Indium and Gallium.
16. A MOSFET fabrication **process** comprising:
- (a) selecting a semiconductor substrate having means for electrically isolating
transistors;

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- 1 (b) introducing channel dopants into said substrate in such a way that the
dopant concentration varies significantly in the vertical but not the lateral
direction;
- (c) forming a gate electrode on said semiconductor substrate;
- (d) forming source and/or drain electrodes on said semiconductor substrate, at
6 least one electrode forming a Schottky or Schottky-like contact to said
semiconductor substrate.
17. The MOSFET fabrication **process** of Claim 16 wherein said MOSFET device
fabricated has a channel length of less than or equal to 100 nm.
18. The **product** created by the process of Claim 16.
- 11 19. The **product** created by the process of Claim 17.
20. A MOSFET fabrication **process** comprising:
- (a) selecting a semiconductor substrate having means for electrically isolating
transistors;
- (b) introducing channel dopants into said substrate in such a way that the
6 dopant concentration varies significantly in the vertical but not the lateral
direction;
- (c) growing a thin gate insulating layer on said semiconductor substrate and
depositing a thin conducting film on said insulating layer;
- (d) patterning and etching said conducting film to form a gate electrode;
- 1 (e) forming one or more thin insulating layers on one or more sidewalls of said
gate electrode and exposing said semiconductor substrate on one or more
active areas of said MOSFET except for said sidewalls;
- (f) depositing a thin film of metal on all surfaces of said MOSFET;

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1 (g) thermally annealing said MOSFET to form a metal-semiconductor on the exposed surfaces of said semiconductor surfaces;

(h) removing unreacted metal from said MOSFET while leaving said metal-semiconductor alloy in contact with said semiconductor substrate.

21. The MOSFET fabrication **process** of Claim 20 wherein said MOSFET device
6 fabricated has a channel length of less than or equal to 100 nm.

22. The **product** created by the process of Claim 20.

23. The **product** created by the process of Claim 21.

24. A **process** for manufacturing a device for regulating the flow of electrical current comprising:

11 (a) providing a semiconductor substrate having a surface and an interior region, said surface having certain sections designated as predetermined regions;

(b) providing for impurity atoms in said interior region of said semiconductor substrate so that, at least in the area proximal to said predetermined regions, the concentration of said impurity atoms does not vary substantially in the
6 direction parallel to said surface of said semiconductor substrate, but does vary substantially in the direction perpendicular to said surface of said semiconductor substrate;

(c) forming, at least in the area proximal to said predetermined regions, a gate electrode; and

1 (d) forming, at least in the area proximal to said predetermined regions, source and drain electrodes which, at least at some point proximal to either edge of said gate electrode, form a Schottky or Schottky-like interface with said semiconductor substrate.

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- 1 25. The **process** of Claim 24 wherein said source and/or drain electrodes are formed
from the group consisting of Platinum Silicide, Palladium Silicide and Iridium
Silicide, and said impurity atoms are selected from the group consisting of Arsenic,
Phosphorous and Antimony.
- 5 26. The **process** of Claim 24 wherein said source and/or drain electrodes are formed
from the group consisting of any of the rare-earth silicides, and said impurity atoms
are selected from the group consisting of Boron, Indium and Gallium.
27. The **process** of Claim 24 wherein said gate electrode has a width not exceeding
100 NM.
- 1 28. The **process** of Claim 27 wherein said source and/or drain electrodes are formed
from the group consisting of Platinum Silicide, Palladium Silicide and Iridium
Silicide, and said impurity atoms are selected from the group consisting of Arsenic,
Phosphorous and Antimony.
- 5 29. The **process** of Claim 27 wherein said source and/or drain electrodes are formed
from the group consisting of any of the rare-earth silicides, and said impurity atoms
are selected from the group consisting of Boron, Indium and Gallium.
30. The **product** created by the process of Claim 24.
31. The **product** created by the process of Claim 25.
32. The **product** created by the process of Claim 26.
33. The **product** created by the process of Claim 27.
- 1 34. The **product** created by the process of Claim 28.
35. The **product** created by the process of Claim 29.

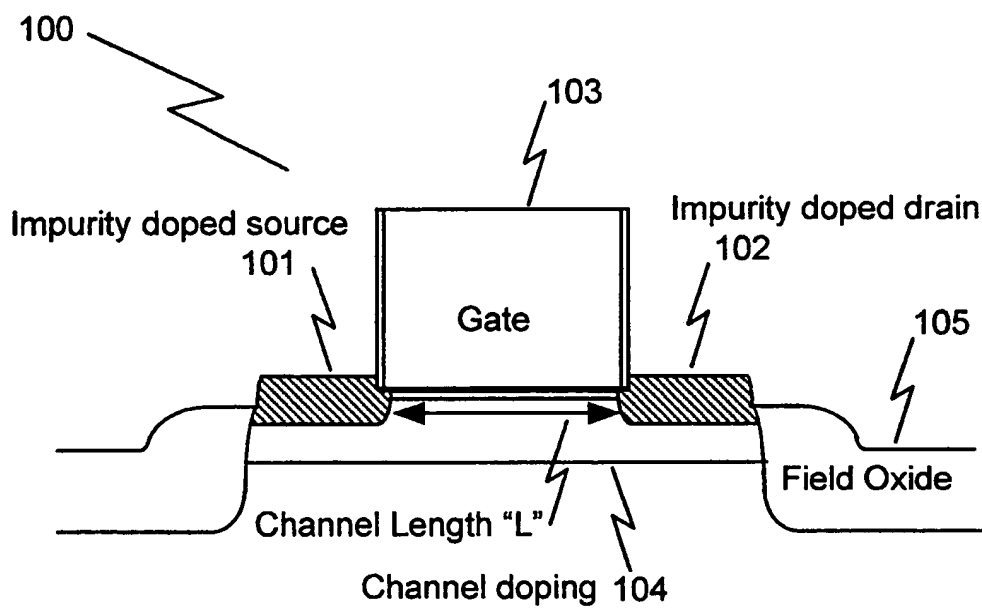
FIG. 1***PRIOR ART***

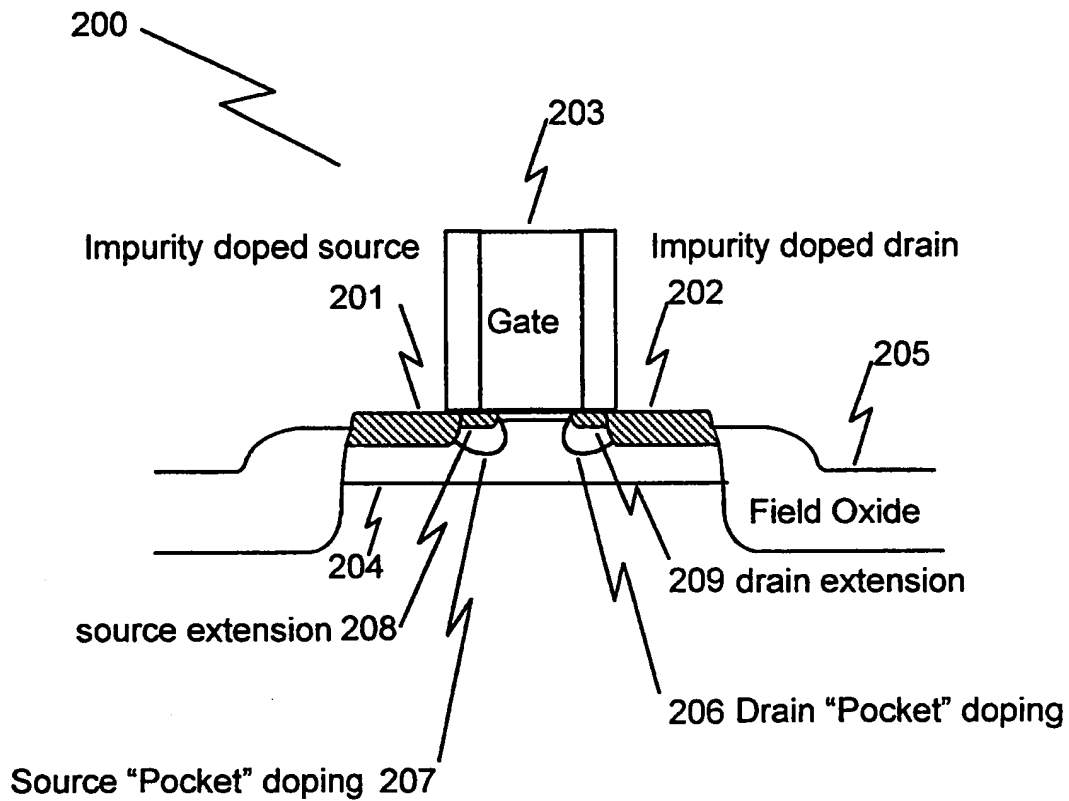
FIG. 2**PRIOR ART**

FIG. 3

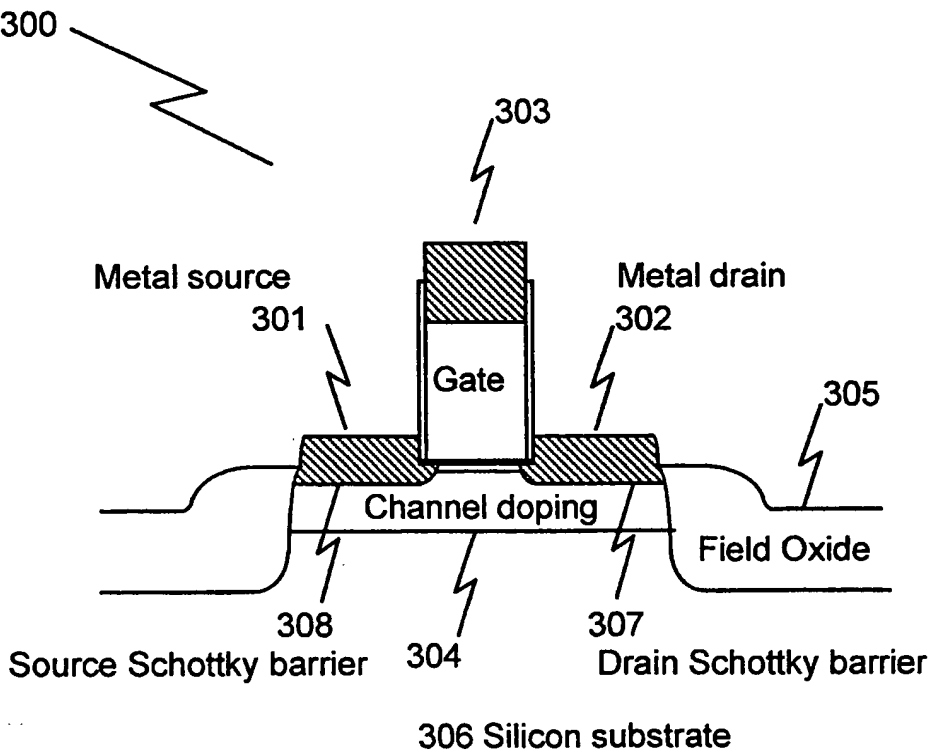


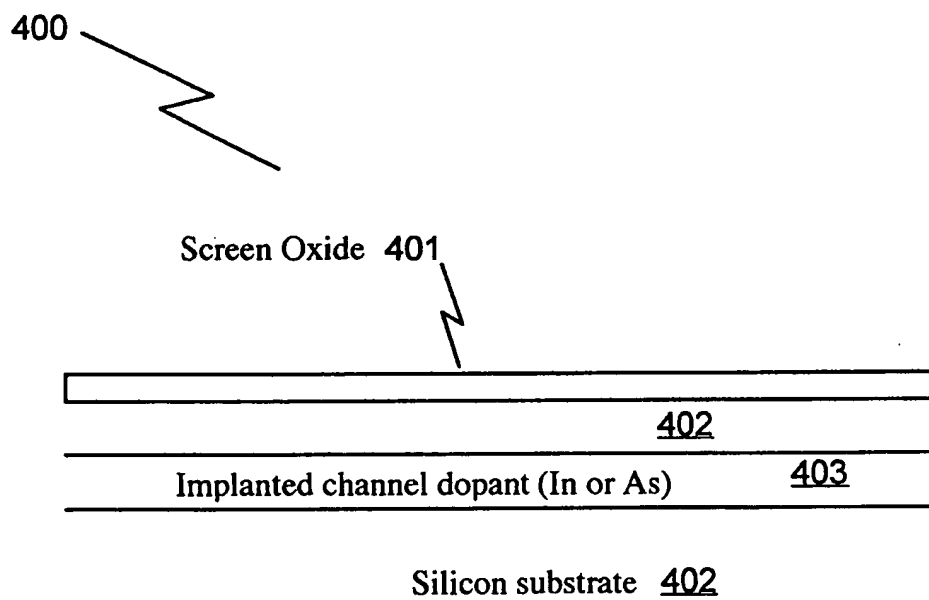
FIG. 4

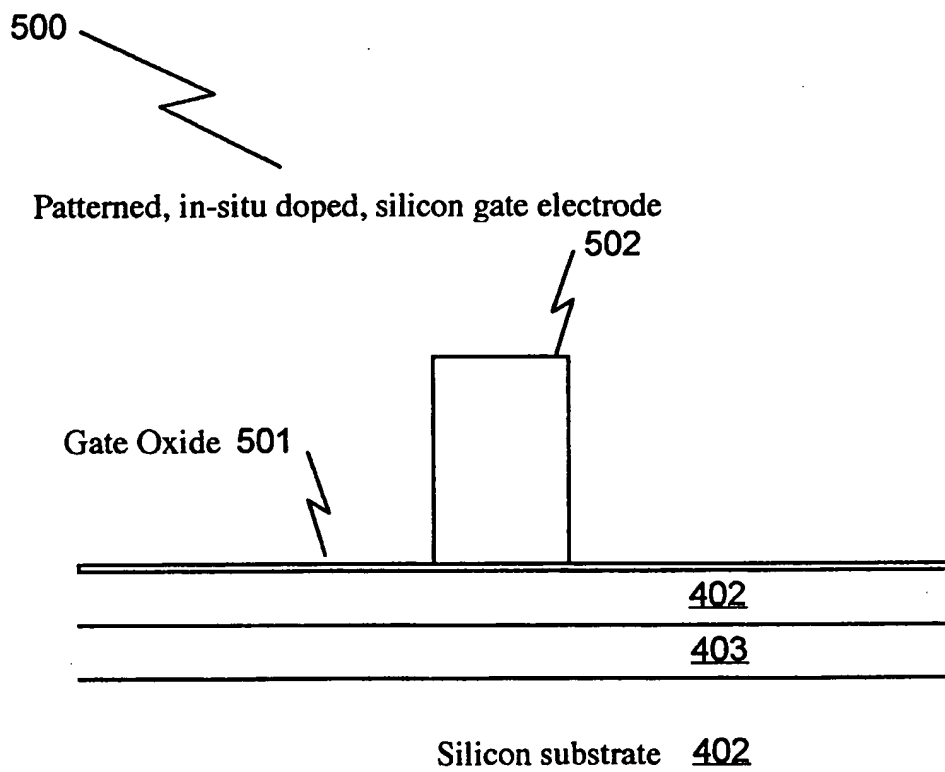
FIG. 5

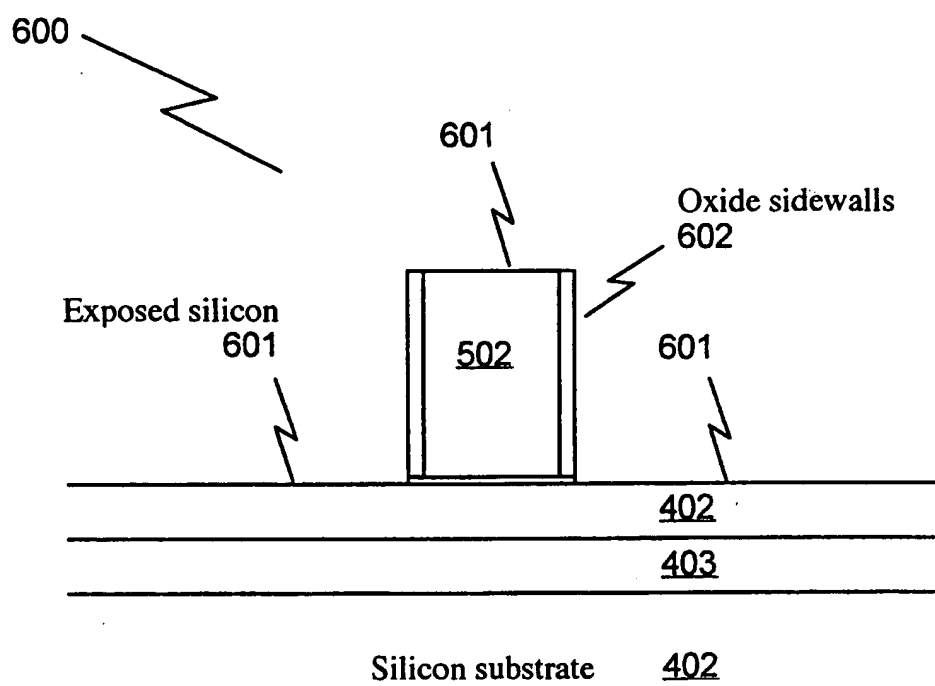
FIG. 6

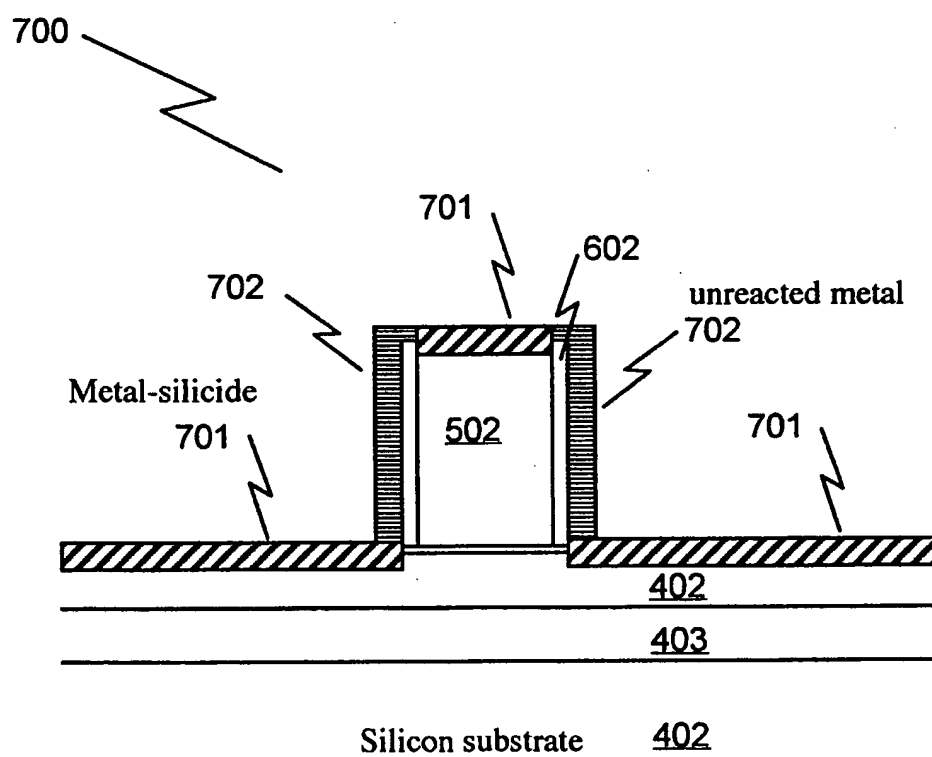
FIG. 7

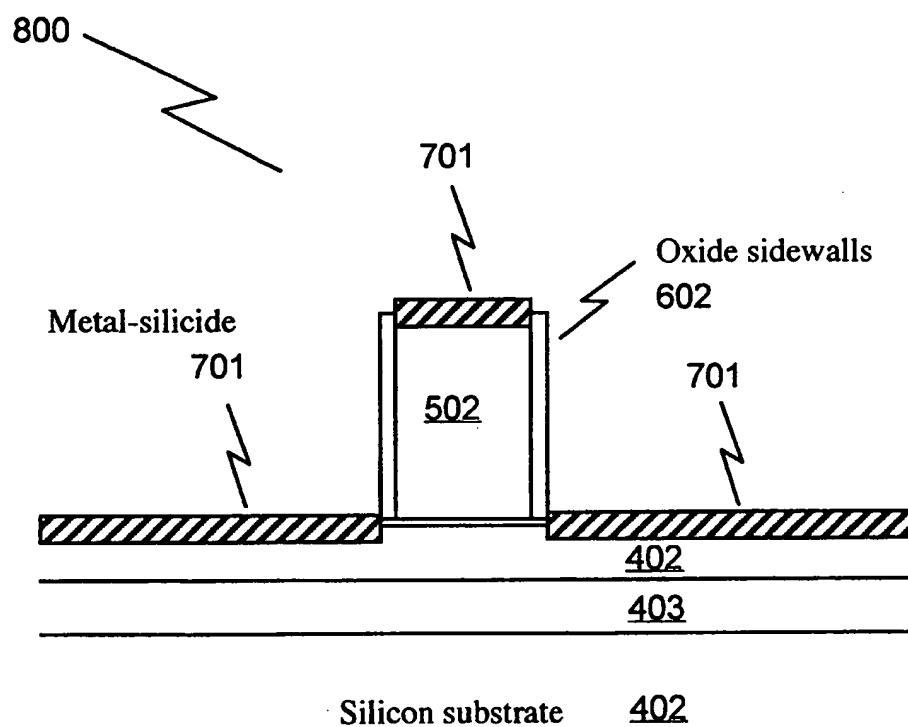
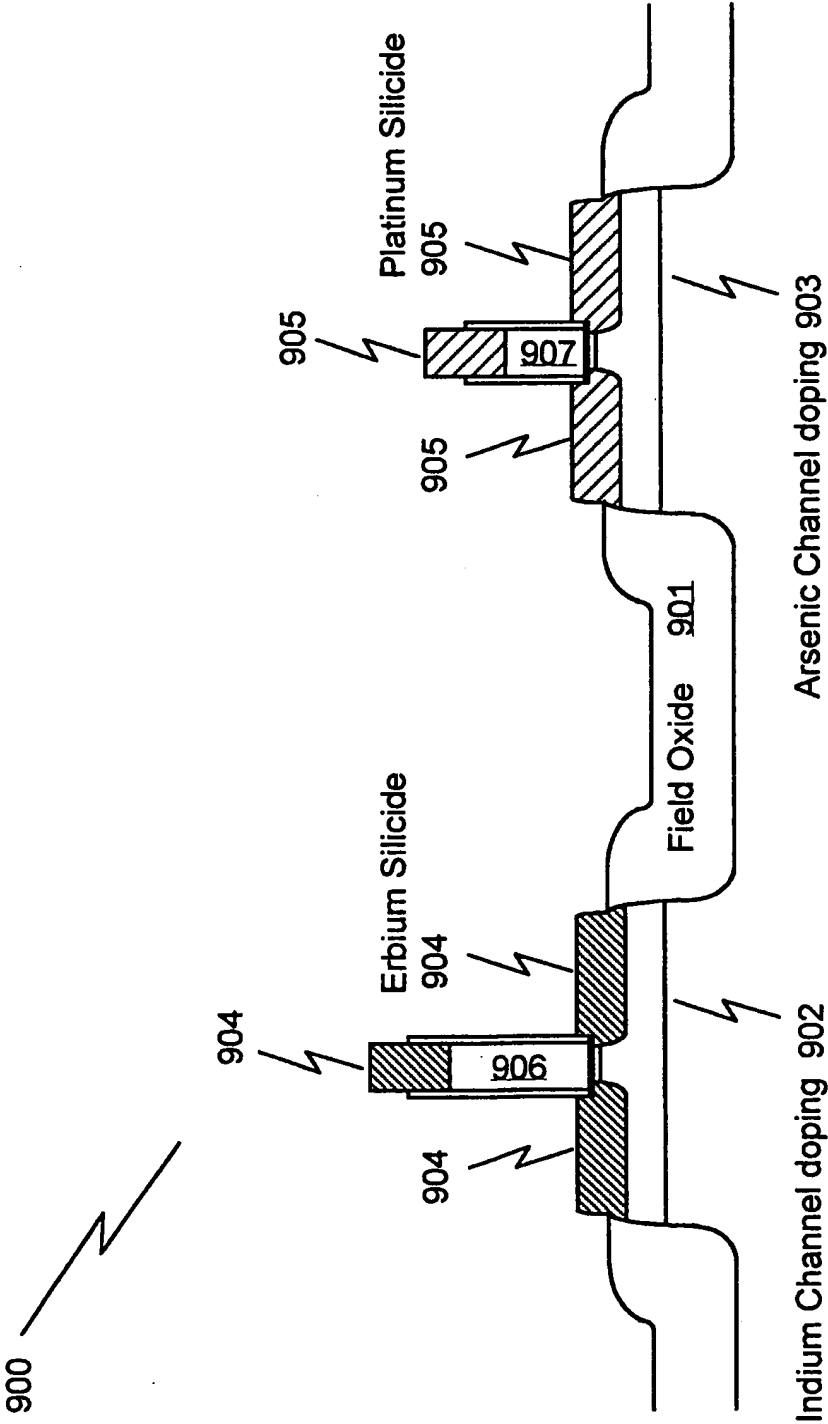
FIG. 8

FIG. 9



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/34082

A. CLASSIFICATION OF SUBJECT MATTER IPC(7) : H01L 21/336; H01L 29/76 US CL : 438/301, 299, 197, 199, 580-583; 257/327, 355, 368, 412 According to International Patent Classification (IPC) or to both national classification and IPC														
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 438/301, 299, 197, 199, 580-583; 257/327, 355, 368, 412 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched NONE Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EAST search terms: schottky, channel, source with drain, implant, silicide, semiconducting, silicon														
C. DOCUMENTS CONSIDERED TO BE RELEVANT														
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.												
X	US 5,801,398 A (HEBIGUCHI) 01 September 1998 (01.09.1998), Figures 5,6,15; col. 9, line 4 through col 10, line 58.	1-3,5,7,9, 10,16,18, 24,30												
----- Y		----- 4,6,8, 11-15,17, 19-23, 25-29, 31-35												
Y,P	US 6,037,605 A (YOSHIMURA) 14 March 2000 (14.03.2000), col. 4, lines 34-42, Figure 7.	4,6,8,17, 19,21,23, 27,33												
Y	US 5,444,302 A (NAKAJIMA et al.) 22 August 1995 (22.08.1995), col 19, lines 59-68.	11-15,25, 26,28,29, 31,32,34,												
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.														
<table border="0"> <tr> <td>* Special categories of cited documents:</td> <td>*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>*A* document defining the general state of the art which is not considered to be of particular relevance</td> <td>*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>*E* earlier document published on or after the international filing date</td> <td>*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>*G* document member of the same patent family</td> </tr> <tr> <td>*O* document referring to an oral disclosure, use, exhibition or other means</td> <td></td> </tr> <tr> <td>*P* document published prior to the international filing date but later than the priority date claimed</td> <td></td> </tr> </table>			* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	*A* document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	*E* earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*G* document member of the same patent family	*O* document referring to an oral disclosure, use, exhibition or other means		*P* document published prior to the international filing date but later than the priority date claimed	
* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention													
A document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone													
E earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art													
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P document published prior to the international filing date but later than the priority date claimed														
Date of the actual completion of the international search 16 FEBRUARY 2001		Date of mailing of the international search report 29 MAR 2001												
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230		Authorized officer <i>Shawn J. Noppe</i> MICHAEL TRINH Telephone No. (703) 308-1782												

INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US00/34082**C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,053,924 A (ROMAN et al.) 11 October 1977 (11.10.1977), col. 5, lines 14-26.	11-15,25, 26,28,29, 31,32,34, 35
X --- Y,P	US 5,079,182 A (IIDEREM et al.) 07 January 1992 (07.01.1992), col. 4, line 26 through col. 8, line 62.	20,22 ----- 21,23
A	US 5,767,557 A (KIZILYALLI) 16 June 1998 (16.06.1998), col. 3, line 5 through col. 4, line 67; Figures 2-8.	9,16,24